WB8-TSL
LORAN C simulator
For frequency reference
12/13/2009

Written by: Paul Swedberg

Introduction
This document describes the simple LORAN C simulator to allow Austron frequency measuring receivers to at least be used for comparison after the North American LORAN C chains are shutdown on 4 Jan 2010. This simulator may be usable by other receivers but has been tested on the following. Austron 2100F, 2100, and 2000.
The system takes a primary reference of 100KC or 1 MC … and converts it to a LORAN C signal with a GRI rate of 60,000.

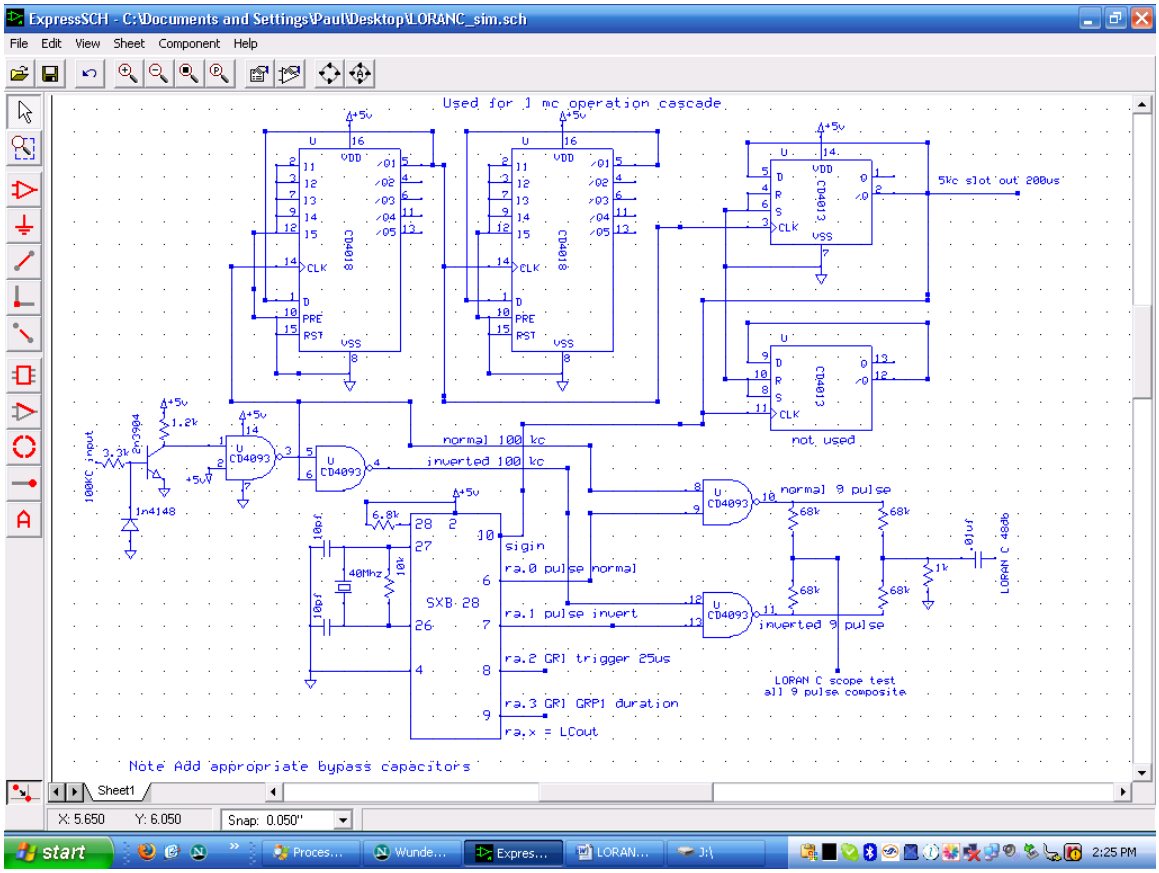
Design principles.
KISS principle.
In that regard every effort has been made to eliminate complexity. This includes transmitted wave shape. Additionally the minimum chip count and very common chips have been used.

Considerations included a pure counter and eprom approach. But since this required quite a few number of table entries it was eliminated. Additionally I wanted to preserve the master reference with the minimum of effect so this essentially is 2 gates and a resistive summer.

This design revolves around the following simplification. That is to consider each Loran Pulse as a time slot of 5KC or 200 us. The pulse slot has 3 possible states. Normal pulse 0 degrees, Inverted pulse or 180degrees, No pulse or silence. By this approach the table drops to 50 entries.
Because LORAN C actually has 2 patterns known as group 1 and 2 this table must be entered twice with the different sequences of normal and inverted pulse phase. Granted the table could be reduced even further. But there is plenty of room in the micro for this so no need to complicate the design.

Schematic of the system.

The schematic is below and consists of 3 sections.
100KC input and shaping
The RISC microprocessor a Ubicom SX B programmed in basic Availble from DigiKey, Mouser, and Parallax approx price $3.95 each.
The pulse assembly and output stage.



Schematic flow

Input shaping
100 KC .5-1 vpp from the local primary reference enters into a 2n3904 transistor to increase the amplitude to roughly a square wave. This goes to a cmos 4093 quad schmitt nand gate to square it up. The output has several uses
It is the 100 KC 0 degree reference for the pulse output
To the cd 4018 counter chain to create the 200 us pulse time slot reference
The next gate to be inverted for the 180 degree pulse output.

Following the divider path the first CD4018 divides by 10 and then feed the CD4013 to be divided by 2 resulting in a 5 KC 50% duty cycle square wave. Though this signal is also feed to a second dividers this is not actually used.
The additional CD4018 is used for dividing a 1 MC reference and you would need to shift the various leads around to use this frequency if a higher frequency is used add divide by 5 or 10 ahead of these dividers.

Microprocessor
The key signal is the 200 us or SIGin signal to the SXB. It is the reference that drives the program.
The SXB runs at 40 MC and as such is much faster then the 200 us slot for the LORAN Pulse. Most of the time the program is waiting for this pulse to go positive then it outputs the pulse type in the next command and then waits for the 200 us pulse to go low before stepping to the next LORAN pulse sequence. This same process is followed even for silent slots.
At the end of the active GRP1 pulses the system waits for 250 200us slots to pass with silence and then goes to the second group sequence. Executes that waits for 250 200us slots to pass and goes back to the start. Changing this count changes the GRI rate.

Other outputs from the Microprocessor use port RA.X a nibble port.
Ra.0 is the gate control for a 0 degree pulse
Ra.1 is the gate control for a 180 degree pulse
Ra.2 is a 25 us scope trigger on the first pulse of master group 1
Ra.3 is a Positive pulse of the entire GRI duration. This will be a length of 50 200us slots or 10 ms followed by the remaining silent 250 X 200 us slots making a total of 60,000us duration.
By carefully measuring Ra.3 you can confirm your GRI rate. This is best done with an accurate delayed sweep scope.

The pulse output assembly

This section is controlled by the microprocessor and consists of the remaining 2 gates from the CD4093.
One gate is the 0 degree pulse
The other is the 180 degree pulse
Ra.0 or 1 control these gates. If both are 0 then a silence is sent.
The output of these gates feed 2 resistive adders.
The first adder assembles the 0 or 180 degree pulses together so that a scope can be used to view the output at approx 2 vpp.

The next adder attenuates the signal by 68,000/1000 ohms and presents a roughly 100 uv signal out to the receiver. The Austron 2100F indicates this to be a 48dbv level. Then the signal goes through a capacitor for DC isolation from the gates and also from the typical receiver preamp voltage on most antenna outputs.

Granted using NAND gates cause an upside down pulse set and dc offset. But this kept everything in 1 simple chip. An alternate arrangement would be inverter and AND gate of even a XOR gate. (Did not have one in the parts bin).

Use of the LORAN C simulator

This system only generates master groups.
The primary reference is input to the LORAN C simulator system and the antenna output is delivered to the Austron. The Austron also has the reference to be compared connected to it as is normal.
Power applied.
Then turn on the Austron and set a GRI of 60,000
The acquire the master.
The system will acquire in 30-300 seconds
Then settle and track in 1-20 minutes.
I am seeing a typical sequence in 1-3 minutes and a frequency offset at track mode of 1 X E-10 or 11^{th} region.
After tracking for 2 hours 1 X E-12. But in reality things drift around at this level. I only have RB sources so I do not really know what the system limit is.