

Evaluation board manual

-MB1500EB16E-

PLL Frequency Synthesizer IC

MB15F7xSP

MB15F7xUL

MB15F8xUL

For BCC Package

The Fujitsu logo consists of the word "FUJITSU" in a bold, red, sans-serif font. Above the letter "I" is a stylized infinity symbol (∞) also in red.

THE POSSIBILITIES ARE INFINITE

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1.0 General Description

The MB1500EB16E is the evaluation board for MB15F7xSP/UL and MB15F8xUL with BCC package. It can evaluate almost performance for PLL.

The loop characteristics can be measured by putting RF/IF VCO and RF/IF loop filter on the board. Each output as RF/IF VCO output and the external input as REF, CLK, Data, LE input pad are prepared. VCO and loop filter are not assembled on the board, so it is flexible.

Regarding CLK, Data and LE input, Fujitsu prepare the software and the cable. The sets can control the data on a PC easily. (The part number of the cable is MB1500EB00A)

The socket for IC is set on the board, because many samples can be changed and evaluated.

2.0 Design Kit

The design kit includes the following items.

- Evaluation board with the socket for BCC package.
- Evaluation board manual

3.0 Set up

1.VCO and Loop filter

RF/IF VCO and RF/IF PLL are assembled. VCO and LPF are not assembled on the board that is supplied.

2.REFin

Connect a signal generator or TCXO to the REF pad. If the TCXO module is used, remove the 51ohm resistor.

3.VCO output

Connect RFVCO output pad to the spectrum analyzer or the modulation domain analyzer.

*SMA connector does not connect to IF VCO output pad.

4.CLK, Data, LE

Connect the output pin of printer port or the special cable through a PC to the pins of CLK, Data and LE.

Fujitsu prepare the special cable for the Fujitsu's software of writing data.

The part number is MB1500EB00A. If you need it, please contact the sales.

5.Vcc and Vp

Connect a DC power supply output to the Vcc and Vp pins.

VCCRF, VpRF, VCCIF and VpIF must supply equal voltage. Even if either RF-PLL or IF-PLL is not used, power must be supplied to both VCCRF, VpRF, VCCIF and VpIF To keep them equal.

It is recommended that the non-use PLL is controlled by power saving function.

6.PLL IC

The socket is attached on the board. It is removed and put a PLL IC. And then IC is suppressed with the socket. Many samples can be measured.

7.Power saving switch

There are two switch. They can control the power saving mode. RF and are separated.

4.0 Device (PLLIC) information

The evaluation board, MB1500EB16E can evaluate the following devices.

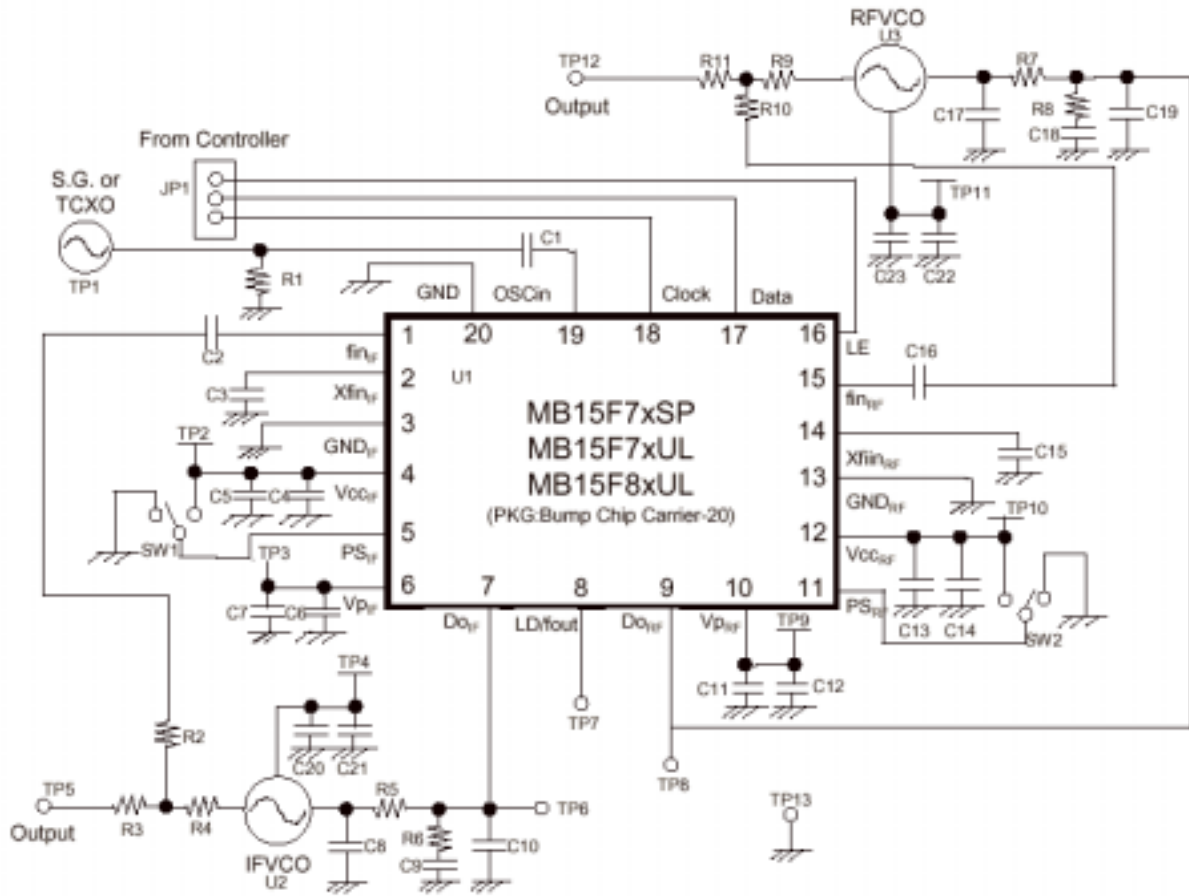
P/N	Data sheet number		Function
	Japanese	English	
MB15F72SP	DS04-21363-2	DS04-21363-2E	1.3/0.35G Integer Dual PLL
MB15F73SP	DS04-21365-1	DS04-21365-1E	2.0/0.6G Integer Dual PLL
MB15F78SP	DS04-21364-2	DS04-21364-3E	2.55/1.2G Integer Dual PLL
MB15F72UL	DS04-21367-1	DS04-21367-1E	1.3/0.35G Integer Dual PLL
MB15F73UL	DS04-21368-1	DS04-21368-1E	2.25/0.6G Integer Dual PLL
MB15F78UL	DS04-21369-1	DS04-21369-1E	2.6/1.2G Integer Dual PLL
MB15F74UL	Under preparing-	Under preparing	4.0/2.0G Integer Dual PLL
MB15F76UL	Under preparing	Under preparing	6.0/1.5G Integer Dual PLL
MB15F83UL	DS04-21371-1	DS04-21371-1E	2.0/0.6G Fractional-N dual PLL
MB15F86UL	DS04-21372-1	DS04-21372-1E	2.5/0.6G Fractional-N dual PLL
MB15F88UL	DS04-21370-1	DS04-21370-1E	2.6/1.2G Fractional-N dual PLL

The data sheets can be done the down load on the web site.

Fujitsu Electrical Device Group web:<http://edevic.fujitsu.com>

5.0 Evaluation board description

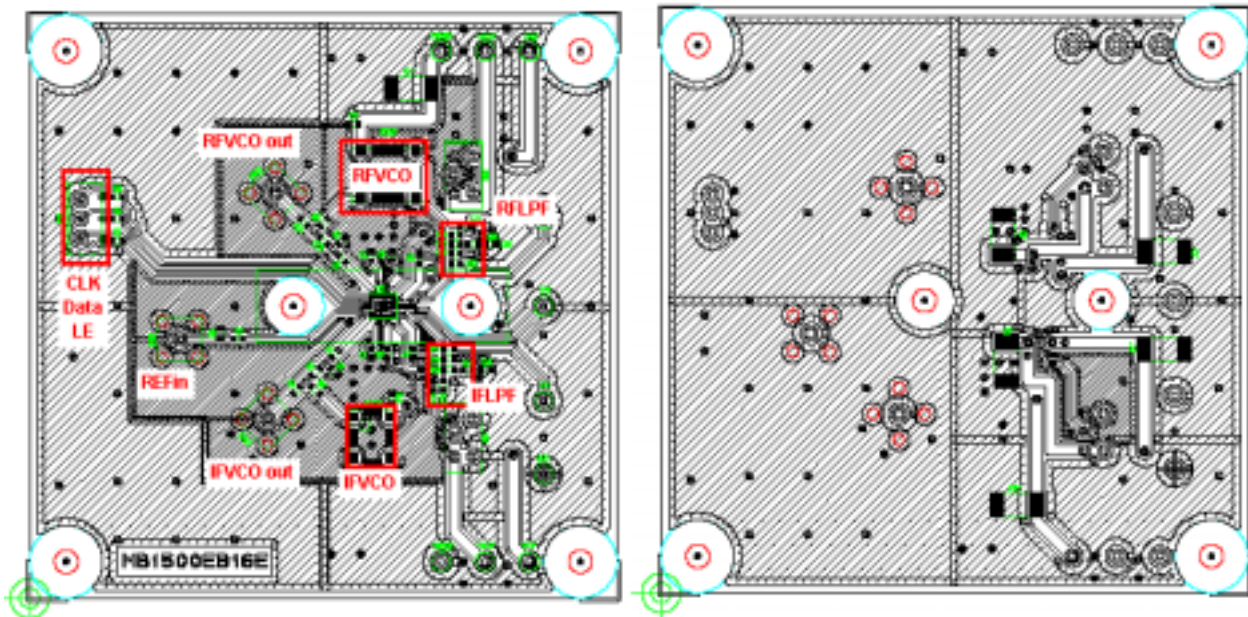
5.1.Board circuit



5.2.Board layout

Top layer

Bottom layer

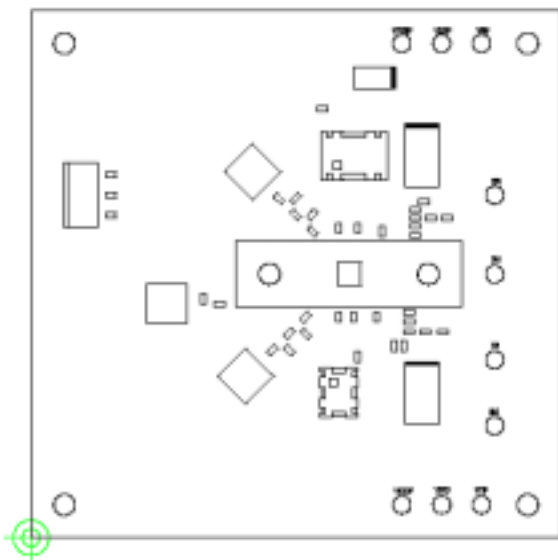


5.2.Components list

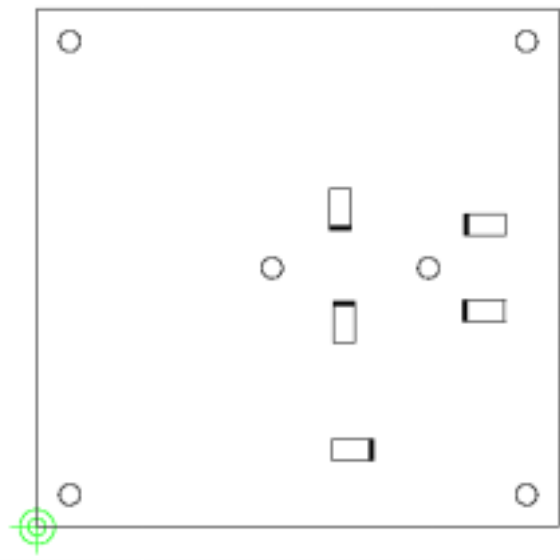
Item	P/N	Description
1	C1,C2,C3,C4,C6,C11,C12, C15,C20,C23	MCH185C102K(ROHM) Cap.1000pF
2	C5,C7,C12,C14,C21,C22	MSVC1C106M(NEC) Cap.10uF
3	R1	MCR03EZHJ510(ROHM) Res.51Ω
4	R2,R3,R4,R9,R10,R11	MCR03EZHJ180(ROHM) Res.18Ω
5	SW1,SW2	G-13AP -
6	JP1	5045-03A -
7	TP2,TP3,TP4,TP6,TP7,TP8 TP9,TP10,TP11,TP12	LC-2-G -
8	U1	PLL IC Open
9	U2	IFVCO Open
10	U3	RFVCO Open
11	C8,C9,C10,R5,R6	IF LPF Open
12	C17,C18,C19,R7,R8	RF LPF Open

5.3.Components layout

Top layer



Bottom layer

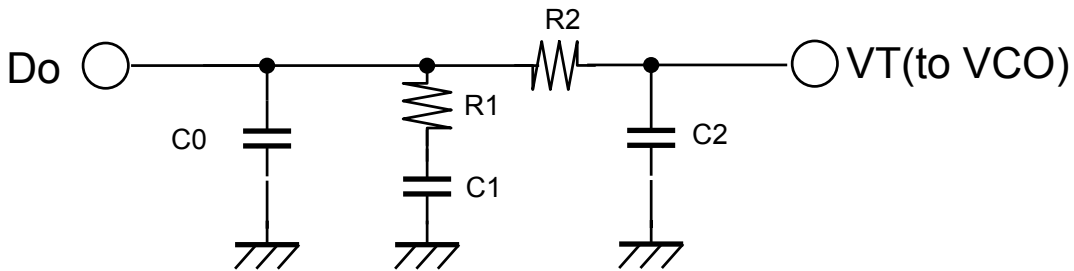


6.0. Typical Test Data

6.1 Measurement Condition

The data is measured under Tri-mode CDMA application.

- Power supply voltage: :Vcc=Vp=2.8V
- Oscillator frequency: :fosc=19.2MHz
- Charge pump current: :ICP=1.5mA
- Comparison frequency: :RF section CDMA) fr=30kHz, PCS) fr=50kHz
- VCO frequency: :RF Dual VCO.(by Fujitsu Media Deveice, VC26-series)
 :RF section---(CDMA) fvco=1052.57MHz to 1077.57MHz
 (PCS)fvco=2113.6MHz to 2173.6MHz
 :IF section-----fvco=360MHz fixed VCO gain :(CDMA)25MHz/V,
 (PCS)50MHz/V
- RF Loop filter



	C0	C1	C2	R1	R2
CDMA	2200pF	0.022uF	510pF	10kΩ	47kΩ
PCS	2700pF	0.027uF	750pF	6.2kΩ	33kΩ

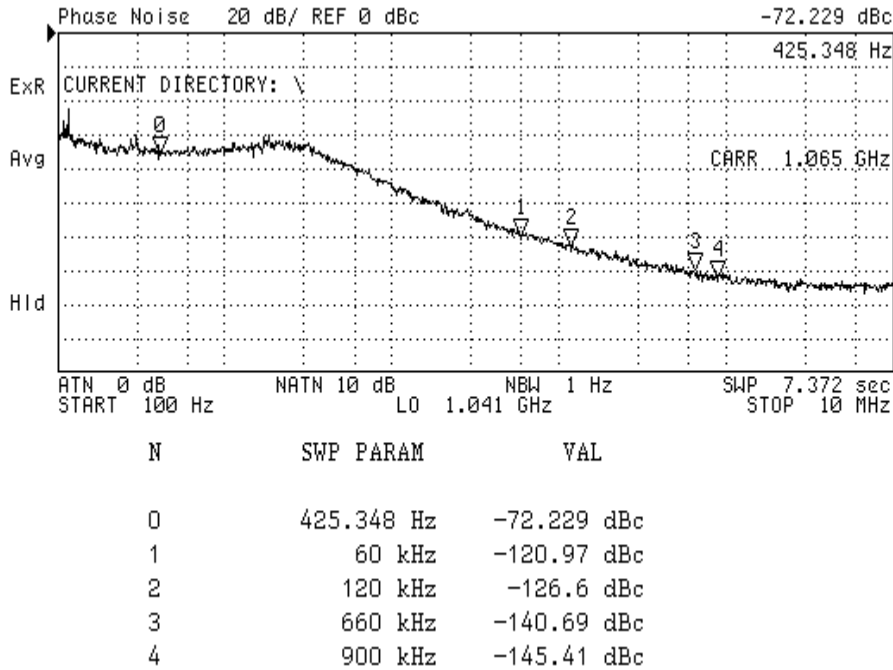
6.2 Typical Measurement Results

Parameter		Measurement	Condition
Lock up time	CDMA	1.52ms	1052.64MHz to 1077.57MHz +/-1kHz
		1.55ms	1077.57 MHz to 1052.64MHz +/-1kHz
	PCS	2.00	2113.6MHz to 2173.6MHz +/-1kHz
		2.02	2173.6MHz to 2113.6MHz +/-1kHz
Phase Noise	CDMA	-120.97dBc/Hz	Offset 60kHz @1065MHz
		-126.6dBc/Hz	Offset120kHz @1065MHz
		-145.4dBc/Hz	Offset900kHz @1065MHz
	PCS	-122.8dBc/Hz	Offset 60kHz @2113.6MHz
		-141.1dBc/Hz	Offset 1.25MHz @2113.6MHz
Spurious	CDMA	-87.6dBc	Offset 30kHz @1065MHz
	PCS	-90.0dBc	Offset 50kHz @2113.6MHz

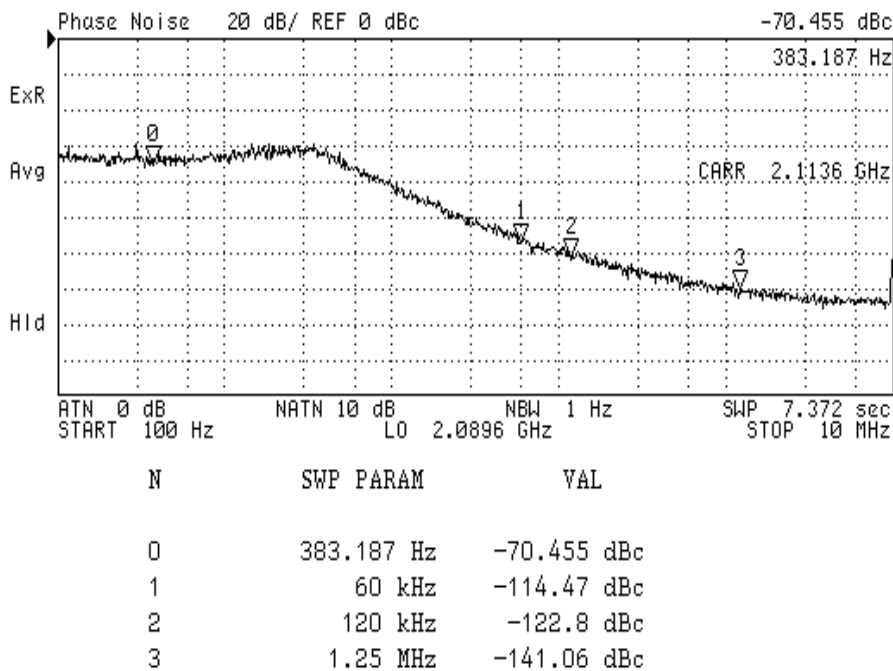
6.3 Measurement wave form

➤ Phase Noise

CDMA band

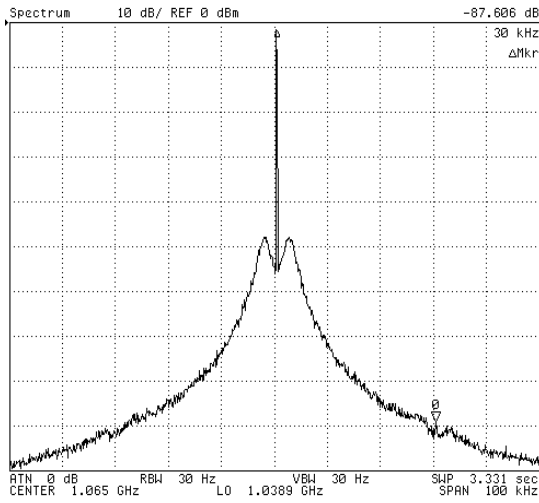


PCS band

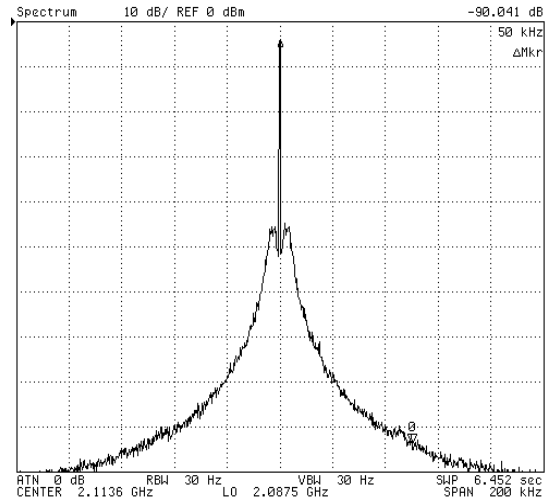


>Spurious

CDMA band

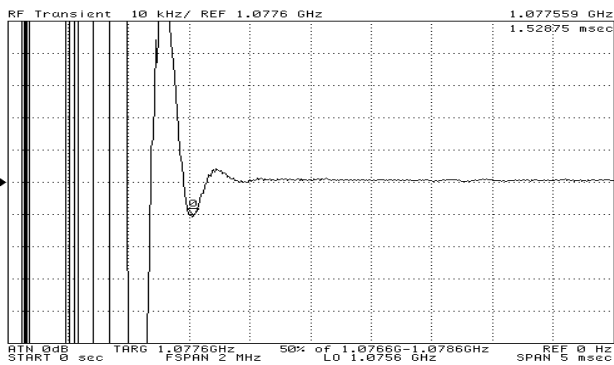


PCS band

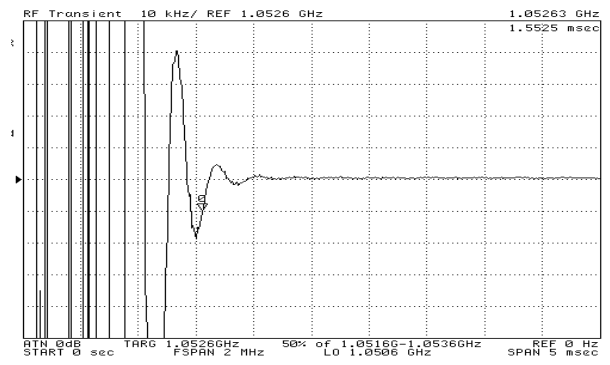


>Lock up time

CDMA band

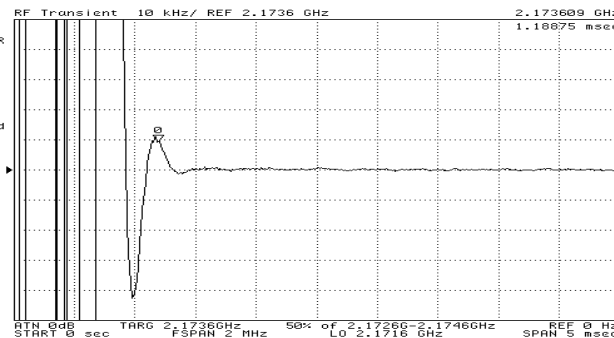


1057.63MHz to 1077.57MHz +/-1kHz

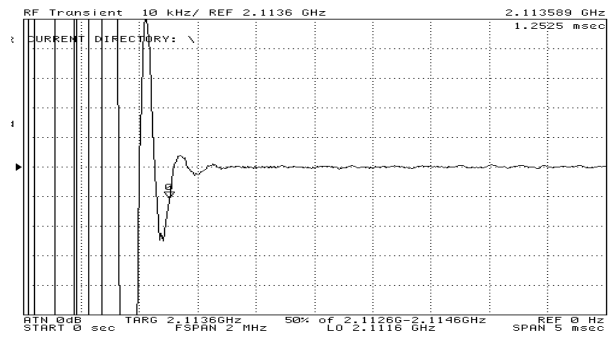


1077.57MHz to 1057.63MHz +/-1kHz

PCS band



2113.6MHz to 2173.6MHz +/-1kHz



2173.6MHz to 2113.6MHz +/-1kHz

7.0 Additional information

Option1

Software and Cable

For writing the serial data, Fujitsu provide the software and special cable.

The software can work under Windows 98SE, Me, NT, 2000 and XP.

MB1500EB00A Kit include

-Cable

-Software

-Manual

Option2

In case of using the other package, TSSOP package, we provide the evaluation board for TSSOP.

MB1500EB16 Kit include

-Evaluation board with the socket for TSSOP package

-Manual.