



# ADG526A/ADG527A — SPECIFICATIONS

Dual Supply ( $V_{DD} = +10.8V$  to  $+16.5V$ ,  $V_{SS} = -10.8V$  to  $-16.5V$  unless otherwise noted.)

Parameter	ADG526A ADG527A K Version		ADG526A ADG527A B Version		ADG526A ADG527A T Version		Units	Comments
	-40°C to +25°C	+85°C	-40°C to +25°C	+85°C	-55°C to +25°C	+125°C		
ANALOG SWITCH Analog Signal Range	V	V	V	V	V	V	V <sub>min</sub>	

Single Supply ( $V_{DD} = +10.8V$  to  $+16.5V$ ,  $V_{SS} = GND = 0V$  unless otherwise noted.)

ADG526A ADG527A K Version	ADG526A ADG527A B Version	ADG526A ADG527A T Version
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# ADG526A/ADG527A

## TIMING DIAGRAMS

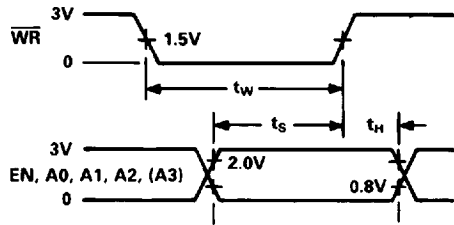


Figure 1.

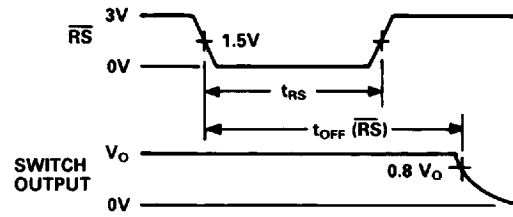


Figure 2.

Figure 1 shows the timing sequence for latching the switch.

Figure 2 shows the Deassert, Pulse Width, and Deassert Time-off.

## TRUTH TABLES

A3	A2	A1	A0	EN	WR	RS	ON SWITCH
X	X	X	X	X	1	1	Retains Previous Switch Condition
X	X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

X = Don't Care

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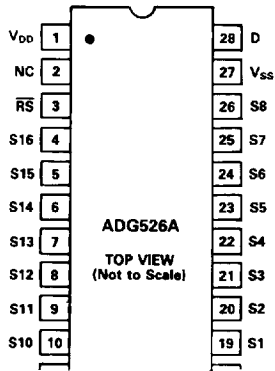
A2	A1	A0	EN	WR	RS	ON SWITCH PAIR
X	X	X	X	1	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

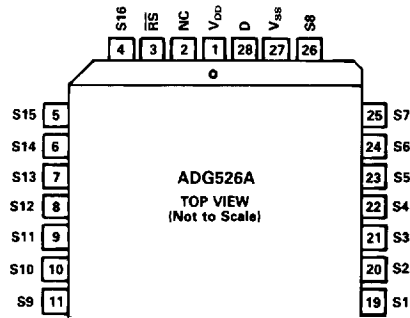
ADG527A

## PIN CONFIGURATIONS

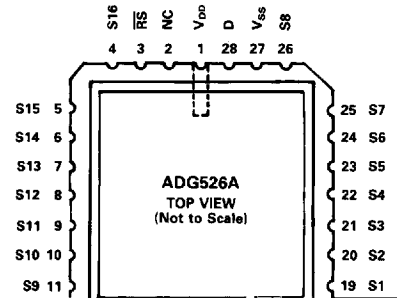
### DIP, SOIC



### LCCC



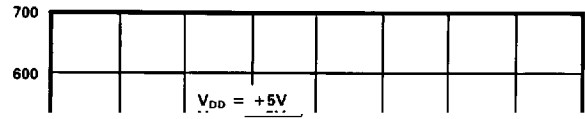
### PLCC



# ADG526A/ADG527A

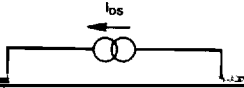
## Typical Performance Characteristics

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.

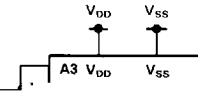
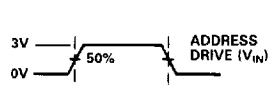


# Test Circuits—ADG526A/ADG527A

TEST CIRCUIT 1  $R_{ON}$

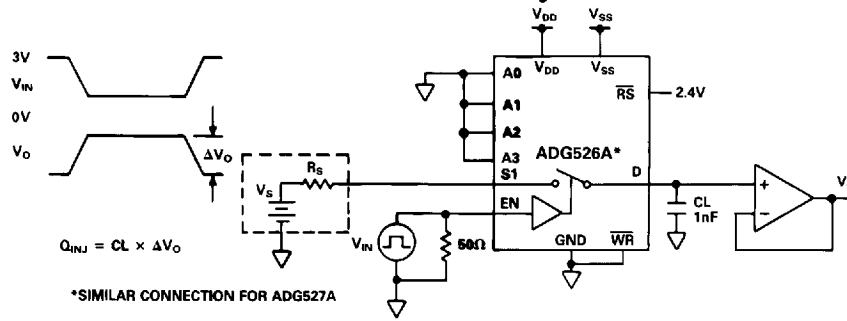


TEST CIRCUIT 6 SWITCHING TIME OF MULTIPLEXER,  $t_{TRANSITION}$



# ADG526A/ADG527A

## TEST CIRCUIT 11 CHARGE INJECTION



### TERMINOLOGY

$R_{ON}$  Ohmic resistance between terminals D and S

$t_{OFF} (EN)$

Delay time between the 50% and 10% points of the digital input and switch "OFF" condition

D-Transition between the 50% and 100% points of



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Datasheets for electronic components.